

Remarks

General:

Claims 1-18 are pending in the application. Claims 1-18 are rejected.

35 U.S.C. § 102 rejections:

Claims 1, 5-6, 10-12, 15-16, and 18 are rejected as anticipated under 35 U.S.C. § 102(b) by U.S. Patent Application No. 2002/0120829 (Murakami '829). The rejection is traversed.

Murakami shows a memory control apparatus in which memory access commands are sent from the CPU 3, through internal buses 16, 17, to a memory access address decoder 22 and a memory access command decoder 23, par. [0069]. From there, the memory access commands pass either via address/data I/O control unit 24, par. [0070] or directly (access control signals 25, par. [0067]) to memory 2. Read and write data are passed by a data path 27, par. [0070], directly between an internal data bus 15 and the I/O control unit 24. However, instructions read from memory are passed from the I/O control unit 24 to the data bus 15 via an instruction prefetch buffer 30-33, Buf4, Buf8, BufC in Fig. 1, 157, 158, 159 in Fig. 8, instead of via the data path 27. The directions of flow are shown by the arrows in Figs. 1 and 8. Flow through the instruction prefetch buffers is entirely unidirectional, from the memory 2 (via the I/O control unit 24) to the CPU 3 (via the internal data bus 15).

The present invention, in contrast, provides buffering "to buffer data between the memory controller and system memory" (claim 1); "interposing a buffer between said system memory bus [connected to system memory] and the memory controller" (claim 12); and "means for buffering data between [the memory] controller and system memory" (claim 18). The buffer is used for "read and write operations" between the memory controller and system memory, and to this end is connected by a "bidirectional data bus" (claims 1 and 18) to the memory controller.

The two systems are fundamentally different. Murakami '829 provides a prefetch buffer that bypasses the data path 27 from the memory controller (at I/O control unit 24) to the internal data bus 15. That is between the CPU and the memory controller, on the opposite side of the memory controller from the memory. Murakami '829 does not show or suggest buffering between the memory controller and the memory, as required by claims 1, 12, and 18, and the present invention is believed to be both novel and non-obvious over Murakami '829.

There is thus no disclosure or suggestion in Murakami '829 of a memory control apparatus or a method for data transfer between a memory controller and a system memory bus connected to system memory as claimed in claims 1, 12, and 18, and claims 1, 12, and 18 are believed to be not only novel but also non-obvious over Murakami '829.

Claims 5-6 and 10-11 are dependent from claim 1 and claims 15-16 are dependent from claim 12 and, without prejudice to their individual merits, are deemed allowable over the cited references for at least the same reasons as claims 1 and 12.

In addition, with reference to claim 11, the examiner asserts that Murakami '829 shows "the buffer comprises: multiple data and control interfaces to system memory, one to interface with each independent portion of system memory." However, the examiner cites only to paragraph [0070], which does not mention the buffer at all, and to items 4 (the bus controller unit as a whole), 24 (the I/O controller), and 200 (the memory as a whole). In fact, there is no suggestion in Murakami '829 of multiple interfaces between the buffer and the memory. There is a single bidirectional interface (probably data) and a single unidirectional interface (probably command) from the I/O controller 24 to the external memory 2, 200, plus the access control strobe and write enable signals 25. There is one unidirectional data path from the I/O controller 24 to the buffer at 31.

In addition, with reference to claim 12, the examiner asserts that Murakami '829 shows "decoding in said buffer the memory interface control commands," and cites to the instruction decoding facility in par. [0028]. What par. [0028] actually says is:

It may be preferable to incorporate an instruction decoding facility to either the instruction buffer or the buffer controller circuit to decode the instructions stating prefetch of instructions into the instruction buffer. It can be determined thereby whether or not the instruction prefetched into an instruction buffer is a branch instruction. When the prefetched instruction is a branch, the number of instructions that may be wasted if prefetched can be reduced by suspending the prefetching of following instructions.

Read as a whole, that paragraph clearly describes decoding the instructions that have been prefetched, in order to see whether they include a branch instruction. There is no disclosure or suggestion in Murakami '829 of decoding memory interface control commands in the buffer.

In addition, with reference to claim 15, the examiner asserts that Murakami '829 shows "controlling read and write operations to said system memory with the decoded memory interface control commands originating in the memory controller and decoded in the buffer," but cites only to "signals originating in from the instruction executing unit" in par. [0032]. It is respectfully pointed out that the "instruction executing unit" is part of the data processor distinct from the "bus controller," par. [0032], lines 7-11. Comparing paragraph [0032] with Fig. 8, with which the examiner is attempting to combine it, the "instruction executing unit" is clearly the CPU 3. Thus, the interface control commands in Murakami '829 do not originate in the memory controller 20, 24, but in the memory access command generator 18. With reference to "decoded in the buffer" the above discussion of par. [0028] applies *a fortiori*.

With reference to claim 16, the examiner asserts that Murakami '829 shows "fanning memory address information" but cites no support for that assertion. As far as applicants can determine, Murakami '829 nowhere mentions or suggests fanning memory address information.

For these reasons also, claims 11, 12, 15, and 16 are deemed novel and non-obvious over the cited reference.

Reconsideration and withdrawal of the rejections under 35 U.S.C. § 102 of claims 1, 5-6, 10-12, 15-16, and 18 are requested.

35 U.S.C. § 103 rejections:

Claims 2-4 and 13-14 are rejected as obvious over Murakami '829 in view of U.S. Patent No. 6,839,806 (Murakami '806).

Claims 2-4 and 13-14 are dependent from claims 1 and 12, and it is noted that Murakami '806 is relied on only for the additional features of claims 2-4 and 13-14. Without prejudice to their individual merits, claims 2-4 and 13-14 are deemed allowable over the cited references for at least the same reasons as claims 1 and 12 are allowable over Murakami '829 alone.

In addition, however, it is respectfully pointed out that it would not have been obvious to add the tag buffer of Murakami '806 to the apparatus of Murakami '829. As noted above, the buffers of Murakami '829 are instruction prefetch buffers. The contents of prefetch buffers are never altered, and never written back to memory, so the sort of tag tracking with which

Murakami '806 is concerned would be totally unnecessary, and totally useless, to the apparatus of Murakami '829.

Further, with reference to claims 2 and 13, there is no suggestion in Murakami '806 of a tag buffer to buffer data between a memory controller and system memory. The examiner refers to the "cache tag buffer 270," but it is clear from the functional description in columns 4 to 6 that this "cache tag buffer 270 for storing a part of a cache tag memory 260" (abstract, lines 1-2) is in fact a cache, not a buffer. (It is perhaps called "buffer" because "cache tag memory cache" would have been a little confusing.)

With reference to claim 3, Murakami '829 does not disclose "a tag control input signal designating said second buffer as the tag buffer." Since the examiner concedes that Murakami '829 does not disclose the second buffer, it would be logically impossible for Murakami '829 to disclose an input signal special to that second buffer. The "flags" to which the examiner refers merely indicate whether the instruction in each buffer is valid or not, par. [0021], and the "intrinsic values" to which the examiner refers are "intrinsic values that a plurality of lower bits in each instruction address may have," that is to say, address offsets to identify the order of the prefetched instructions (the process is described in more detail in par. [0080]).

Claims 7-8 are rejected as obvious over Murakami '829 in view of U.S. Patent application No. 2003/0177320 (Sah et al.) Claims 7-8 are dependent from claim 1, and it is noted that Sah is relied on only for the additional features of claims 7-8. Without prejudice to their individual merits, claims 7-8 are deemed allowable over the cited references for at least the same reasons as claim 1 is deemed allowable over Murakami '829 alone.

Claim 9 is rejected as obvious over Murakami '829 in view of U.S. Patent application No. 2004/0117566 (McClannahan et al.). Claim 9 is dependent from claim 1, and it is noted that McClannahan is relied on only for the additional features of claim 9. Without prejudice to its individual merits, claim 9 is deemed allowable over the cited references for at least the same reasons as claim 1 is deemed allowable over Murakami '829 alone.

In addition, however, the examiner is reminded that the buffers of Murakami '829 are instruction prefetch buffers. It would not be obvious to add McClannahan's tag handling to Murakami '829, because Murakami '829 has no need nor use for the sort of request tracking that McClannahan's tags are intended to mediate.

Claim 17 is rejected as obvious over Murakami '829 in view of U.S. Patent application No. 2003/0163776 (Prasad). Claim 17 is dependent from claim 12, and it is noted that Prasad is relied on only for the additional features of claim 17. Without prejudice to its individual merits, claim 17 is deemed allowable over the cited references for at least the same reasons as claim 12 is deemed allowable over Murakami '829 alone.

In addition, it is respectfully submitted that it would not have been obvious to add Prasad's interleaving system to Murakami '829, because there is no suggestion that the system of Murakami '829 suffers from "bursts" of "channel impairments such as noise, fading, and jamming," Prasad pars. [0004] and [0003]. Prasad is concerned with "digital communication systems," par. [0002]. It is highly improbable that the problems he faces would occur within the data processing device of Murakami '829, and absent evidence of a problem the extra overhead of interleaving and de-interleaving would be contra-indicated. Further, the examiner's proposed combination of Murakami '829 and Prasad would not result in the invention claimed in claim 17. Claim 17 recites interleaving "read and write operations in sequences of memory operations between the controller and multiple independent portions of system memory." Prasad discloses a different sort of interleaving, bitwise interleaving within a single data frame, for a different and unrelated purpose.

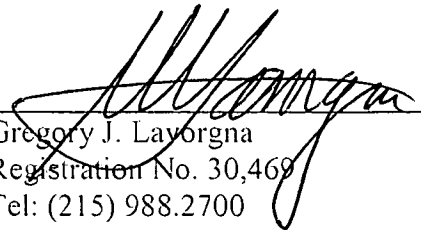
Reconsideration and withdrawal of the rejections under 35 U.S.C. § 103 of claims 2-4, 7-9, 13-14, and 17 are requested.

Conclusion:

In view of the foregoing, all of claims 1-18 are deemed to be allowable. Reconsideration and withdrawal of the examiner's objections and rejections and an early notice of allowance of claims 1-18 are earnestly solicited.

Should the Examiner have any questions or comments regarding Applicants' amendments or response, he is asked to contact Applicants' undersigned representative.

Respectfully submitted,



Gregory J. Lavgorgna
Registration No. 30,469
Tel: (215) 988.2700
Fax: (215) 988.2757
Attorney for Hewlett-Packard Company